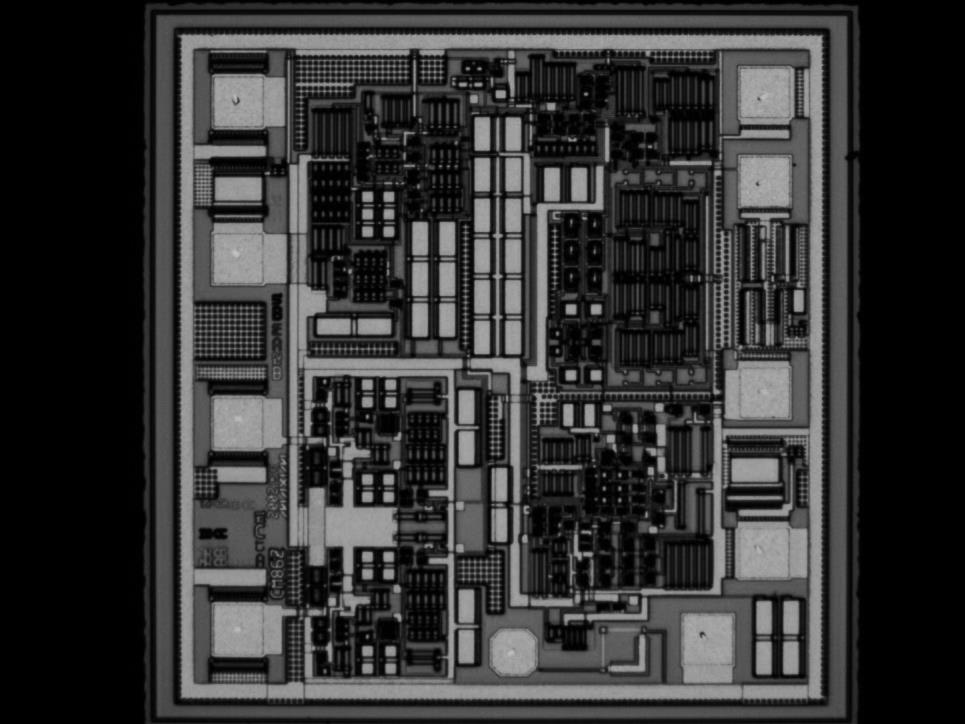
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

****

DRAFT

**.060”**

**CM86Z**

**.061”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: -**

**Mask Ref: CM86Z**

**APPROVED BY: DK DIE SIZE .060” X .061” DATE: 12/5/18**

**MFG: MAXIM THICKNESS .016” P/N: MAX913C/D**

**DG 10.1.2**

#### Rev B, 7/1